AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the above-identified application:

1 (currently amended). A bus isolator for coupling a bus of a first predetermined configuration and signaling protocol (collectively the "first properties") to a peripheral via an I/O of a second predetermined configuration and signaling protocol (collectively the "second properties"), comprising:

a ~~first~~ target interface coupled to the bus according to the first properties and configured to be responsive to a bus controller for transmission of data on the bus;

a ~~second~~ master interface coupled to the I/O according to the second properties;

a controller coupled to and receiving signals from the ~~first and second~~ target and master interfaces;

a memory coupled to the controller for storing signals received from the bus and the I/O; and

a processing element coupled to the controller and the memory and configured to manage ~~for managing~~ the activity of the isolator and to verify the integrity of data contained in the signals received from the master interface, wherein data is transmitted from the ~~I/O~~ target interface to the bus only in response to a data request from the bus controller.

2 (currently amended). The isolator of claim 1 wherein data requested by the bus from the I/O is sent via the ~~second~~ master interface to the memory and the processor, where the integrity of such data is verified and only sent to the bus if of appropriate format so that a defective I/O or a defective peripheral coupled to the I/O cannot capture the bus.

3 (original). The isolator of claim 1 wherein the I/O is a commercially available I/O such that the second properties are standard-off-the-shelf properties.

4 (original). The isolator of claim 1 wherein the bus is a commercially available bus such that the first properties are standard off-the-shelf properties.

5 (currently amended). The isolator of claim 1 wherein the memory comprises an isolation memory, having a first portion wherein data is received from the ~~first~~ target interface and a second portion where data is received from the ~~second~~ master interface.

6 (original). The isolator of claim 5 wherein the memory further comprises a program memory and a flash memory.

7 (original). The isolator of claim 1 wherein the processing element comprises a state machine, a simple controller, a microprocessor, a digital signal processor or a combination of first and second lock-step processors.

8 (currently amended). An electronic system operating in response to a bus controller, the electronic system comprising:

multiple peripherals;

multiple COTS I/O elements, each coupled to one of the peripherals for passing signals to and from the one of the peripherals;

multiple isolation elements, each coupled to at least one of the COTS I/O elements for passing signals to and from the at least one COTS I/O element;

a bus coupled to the multiple isolation elements for sending and receiving signals to and from the peripherals via the isolation elements and the COTS I/O elements; and

wherein each isolation element comprises:

a target interface coupled to the bus for receiving commands from the bus controller and passing valid data requested by the bus controller from the peripheral to the bus;

a master interface coupled to the at least one COTS I/O element for passing commands received from the bus to the peripheral and data requested from the peripheral back to the bus;

a controller coupled to the target interface and the master interface for controlling command and data flow there between;

a memory coupled to the controller for receiving commands and data from the bus and data from the at least one COTS I/O element; and

a processing element coupled to the memory and the controller and configured to manage ~~for managing~~ command and data flow between the bus and the at least one COTS I/O element such that the integrity of data contained in the signals received from the master interface is verified, and such that a signal from the at least one COTS I/O element is only transmitted to the bus in

response to command received from the bus controller allowing such transfer.

9 (original). The system of claim 8 wherein the memory comprises an isolation memory having one part coupled to the at least one COTS I/O element for receiving data transfer therefrom and another part coupled to the bus for receiving command and data transfer therefrom.

10 (original). The system of claim 9 wherein the memory further comprises program memory containing programs for execution by the processor and flash memory for containing configuration data for the isolation element.

11 (original). The system of claim 8 further comprising a debug port coupled to the processing element.

12 (currently amended). A method for coupling a bus and a peripheral via an isolator, comprising:

determining whether there is a message ~~on the bus~~ for the peripheral;

temporarily storing the message in the isolator;

determining whether the message is for output to the peripheral or input from the peripheral; and

if for output to the peripheral, sending the output to the peripheral; and

if for input from the peripheral;

~~requesting the input from the peripheral;~~

receiving the input from the peripheral and temporarily storing it in the isolator;

checking the input from the peripheral; and

if valid, transferring the input from the peripheral to the bus in response to a request from a remote bus controller operating on the bus; and

if not valid, not transferring the input from the peripheral to the bus.

13 (original). The method of claim 12 further comprising before the first sending step, determining whether the output for the peripheral is in the message or already stored in the isolator.

14 (original). The method of claim 13 wherein if the output for the peripheral is already in the message, further comprising determining whether a bus coupling the peripheral to the isolator is free and if free sending the output to the peripheral and if not free setting an error indicator.

15 (original). The method of claim 13 wherein if the output for the peripheral is already stored in the isolator, further comprising retrieving the stored output and determining whether a bus coupling the peripheral to the isolator is free and if free sending the output to the peripheral and if not free setting an error indicator.

16 (original). The method of claim 12 wherein the checking step comprises determining whether the input from the peripheral is timely and valid and if timely and valid

sending the input from the peripheral to the bus and if not timely and valid setting an error indicator.

17 (original). The method of claim 16 further comprising after the sending step, checking to see whether the sending step was successful.

18 (original). The method of claim 12 further comprising after the transferring step, checking to see whether the transferring step was successful.